AEC LAB REPORT – 6

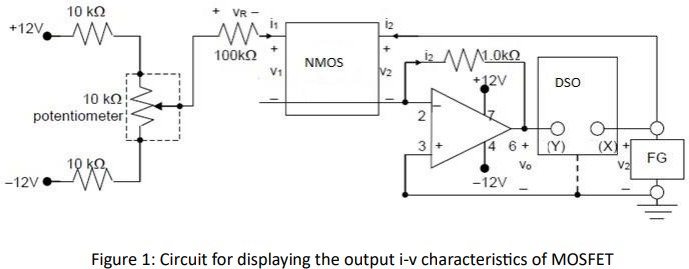
# MOSFET: I-V and Voltage transfer characteristics (VTC)

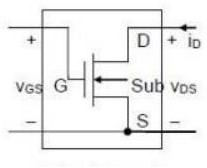
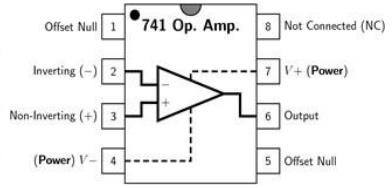
***NAME:*** *Khyathi Sri Basireddy*

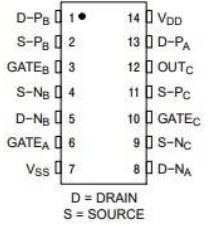
***ROLL NO****: 2023102065*

***TABLE NO: 9***

# ID vs VDS characteristics





### Input parameters:

Channel 1 – D terminal of NMOS Channel 2 – Output of OpAmp (Vo)

WaveGen - Wave – Sine Wave

f = 100 Hz

Vpp = 8V Offset = 4V

From the given circuit, we can see that V2 = VDS

I2 = ID

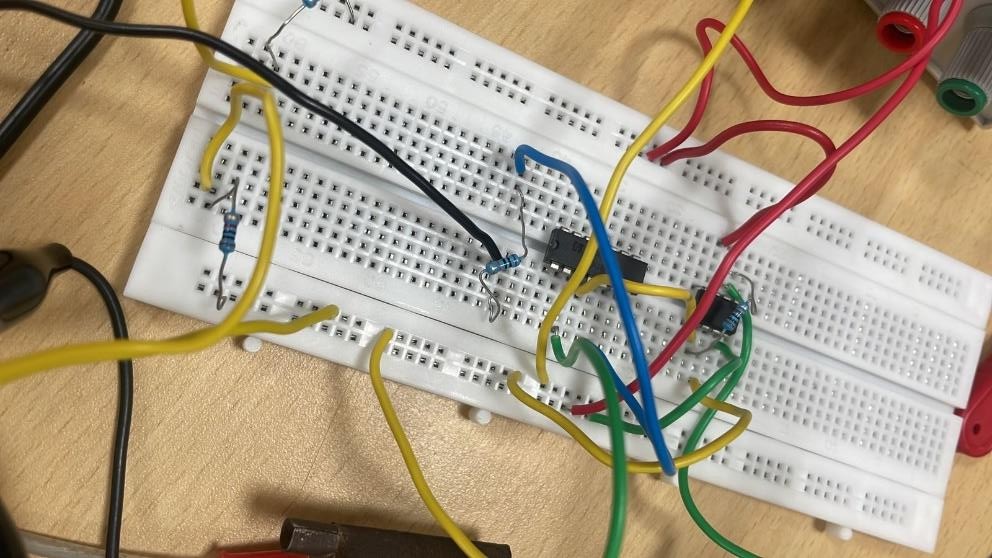
RO = 1k ohm VOUT = - I2 x RO

Potentiometer Outputs:

Maximum Voltage = 4.8V Minimum Voltage = -4.4V



### Circuit:

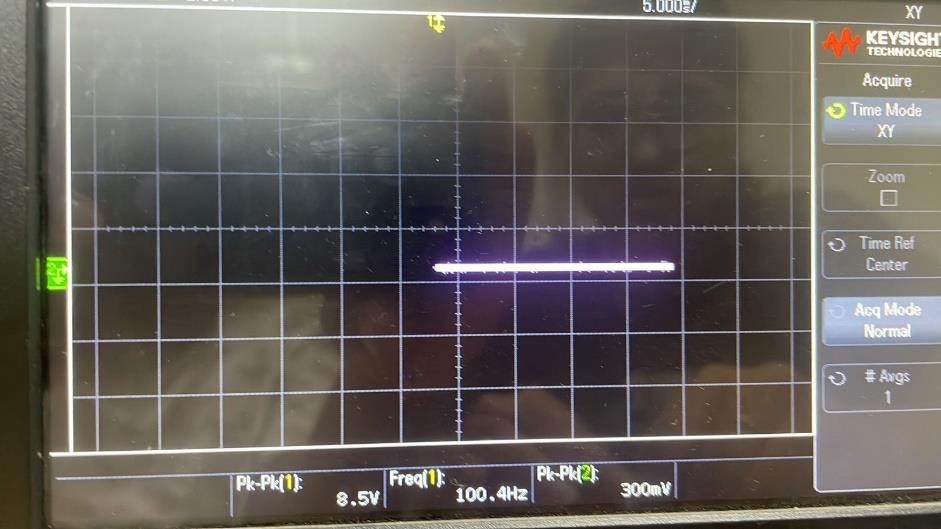


**Start varying the VGS using the potentiometer:**

|  |  |  |  |
| --- | --- | --- | --- |
| **VGS** | **VDS** | **VO** | **ID** |
| 0.2V | 3.99V | -300mV | 300uA |
| 0.3V | 3.99V | -300mV | 300uA |
| 0.4V | 3.98V | -300mV | 300uA |
| 0.5V | 3.98V | -300mV | 300uA |
| 0.6V | 3.99V | -300mV | 300uA |
| 0.7V | 4.00V | -300mV | 300uA |
| 0.8V | 3.99V | -301mV | 301uA |
| 0.9V | 3.99V | -300mV | 300uA |
| 1V | 9.98V | -400mV | 400uA |
| 1.2V | 3.98V | -860mV | 860uA |
| 1.4V | 3.95V | -1.1V | 1.1mA |
| 1.6V | 3.96V | -1.3V | 1.3mA |

|  |  |  |  |
| --- | --- | --- | --- |
| 1.8V | 3.98V | -1.6V | 1.6mA |
| 2V | 3.98V | -1.9V | 1.9mA |
| 3V | 3.95V | -2.65V | 2.65mA |
| 4V | 3.92V | -3.24V | 3.24mA |

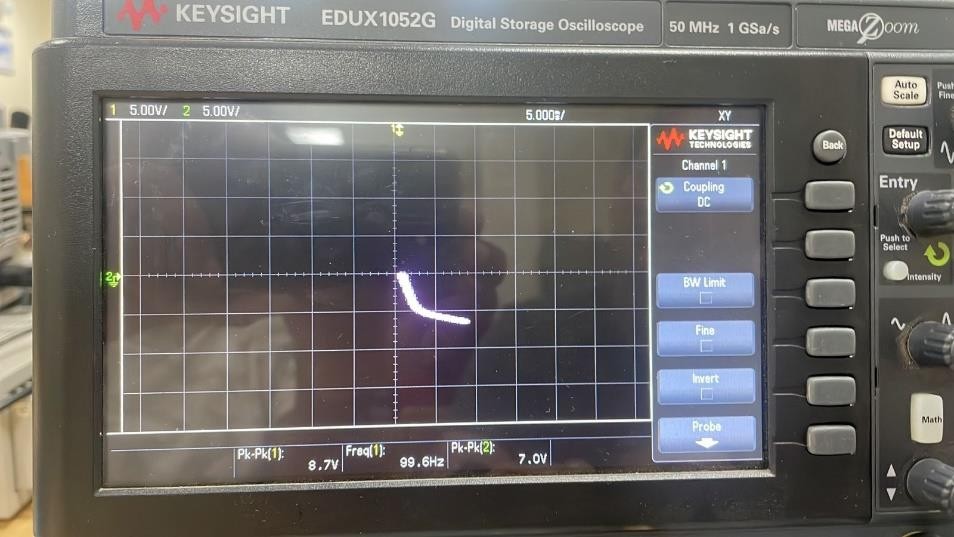
**VGS = 0.3V**



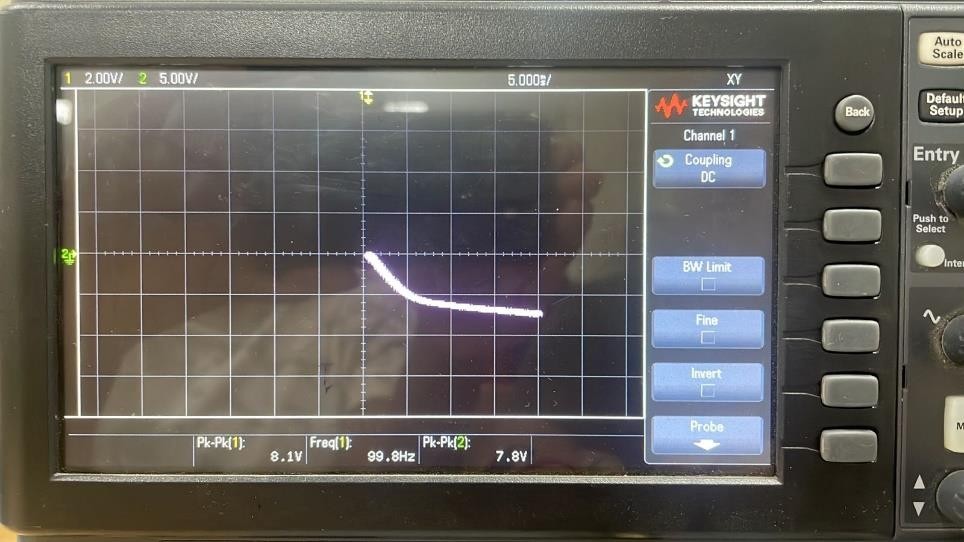
**VGS = 1V**



**VGS = 1.6V**



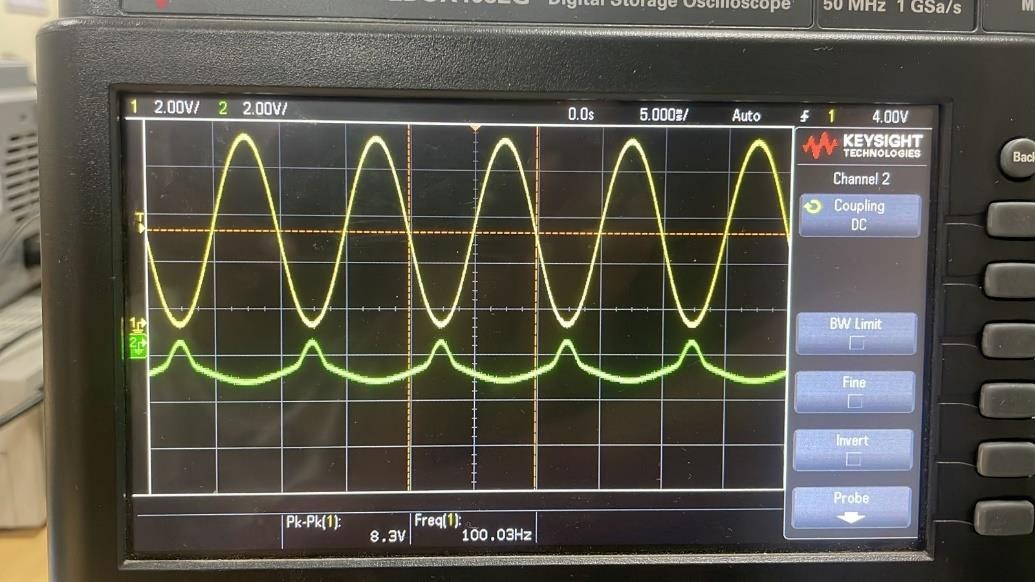
**VGS = 3V**



The Variation of Vout at different VGS: Green – Vout

Yellow - VDS





# ID vs VGS characteristics and parameter extraction

#### Plot of ID vs VGS

To sweep VGS, connect the function generator across the gate terminal and the

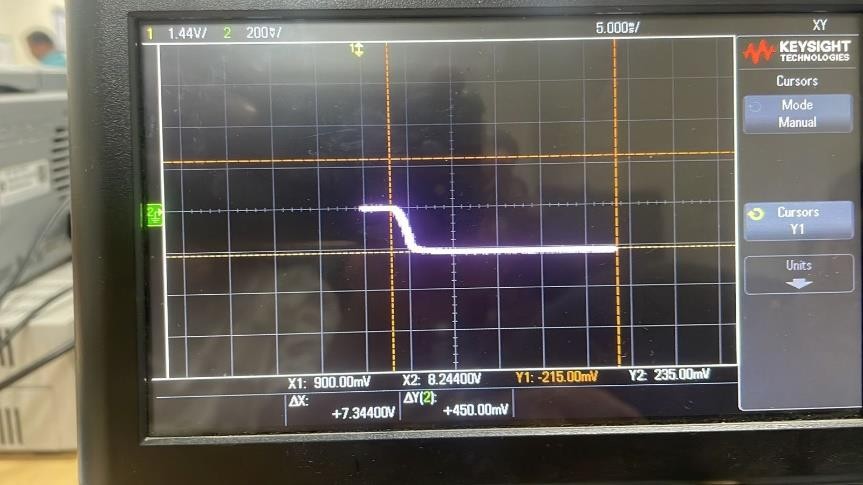
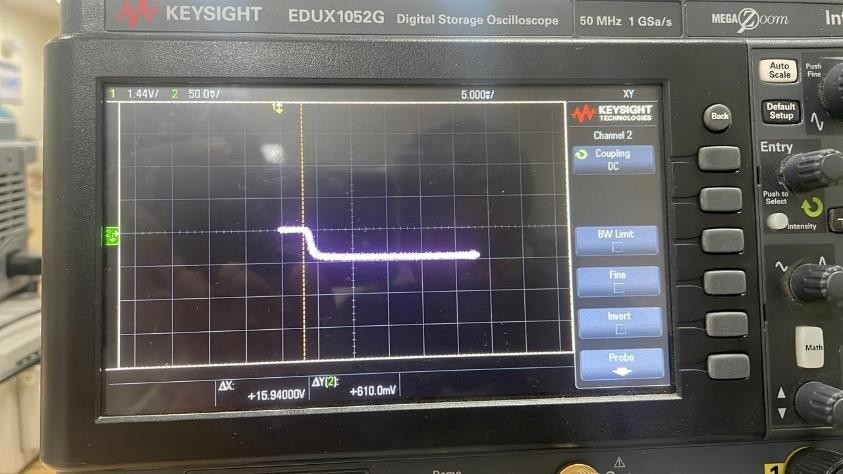
potentiometer across the drain terminal. Give a sinusoidal signal from function generator to the gate.

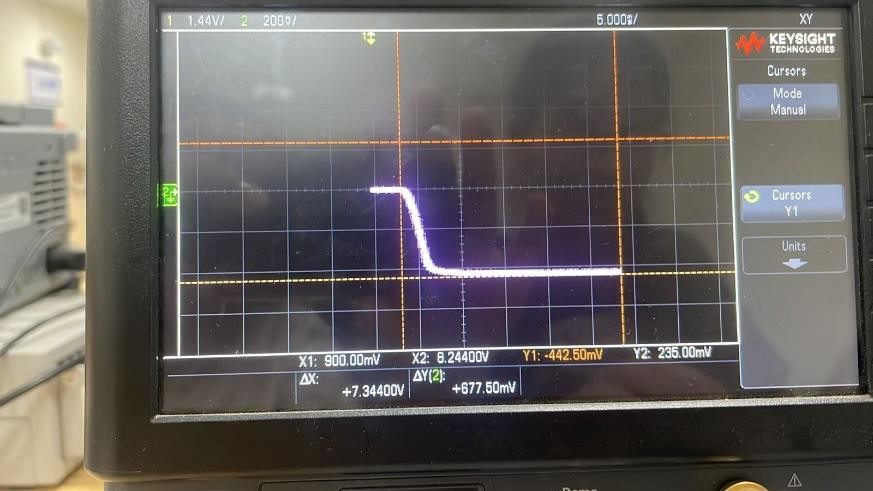
To determine the value of VT of the given NMOS, bias the MOSFET in linear region by using sufficiently smaller value of VDS= 100 mV and plot ID vs VGS by sweeping VGS from 0 to 4 V.

Thus, VDS = 100 mV

We know, VOUT = - ID X RO

|  |  |  |  |
| --- | --- | --- | --- |
| ***VDS*** | ***VGS*** | ***VOUT*** | ***ID*** |
| 0.1V | 3.99V | -2.1mV | 2.1uA |
| 0.5V | 3.99V | -5.15mV | 5.15uA |
| 1V | 3.97V | -9.925mV | 9.925uA |
| 2V | 4.00V | -22.375mV | 22.375uA |
| 3V | 3.98V | -30.475mV | 30.475uA |
| 4V | 3.99V | -37.50mV | 37.50uA |





#### Finding VT

Bias the MOSFET in linear region by using sufficiently smaller value of VDS. The value of VDS is = 100mV

We now try to examine the maximum slope of the curve obtained.

At point (VGS, VOUT) = (1.8, -1.85) we can observe max slope The value of maximum slope = (−2.1 +1.85) / (1.95 − 1.8)

= -1.7(approx).

The points used to measure the slope are (1.8, -1.85) and (1.95, -2.1).

Threshold Voltage (VT) can be obtained when the point of intersection of tangent drawn at max slope point with VGS axis.

Here, VT = 0.72V

1. ***Value of µnCox(W/L)*** Now, all the values we have are VGS = 1.8V

VOUT = -1.85V VT = 0.72V

VDS = 100mV = 0.1V ID = 1.85mA

VGS – VT = 1.8 – 1.72

= 1.08 V

Here,

VGS – VT > VDS

 This means that the transistor is in Linear Mode.

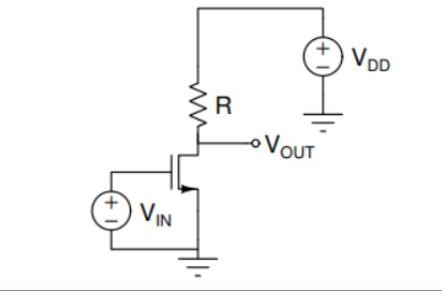


Using the above formula and values,

1.85 x 10-3 = µnCox(W/L) (1.8 – 0.72) (0.1)

µnCox(W/L) = 17.1296 mS/V

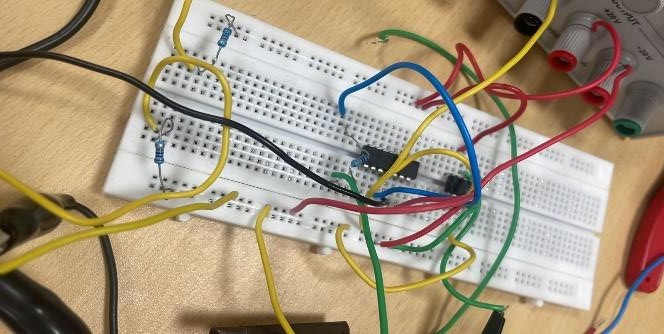
1. ***Large signal analysis and voltage transfer characteristic (VTC)***
2. **Designing the Circuit**



**Input Parameters:** Gate – pin3(input) Source-pin4(ground) Drain - pin5(Vcc) Body - pin7(ground) R = 1k Ohm

VCC = 1.08 Volt

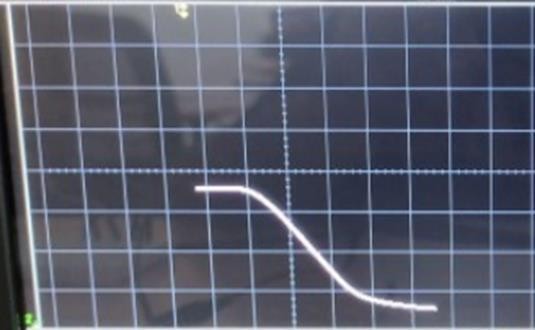
Vin = 2.5 + 2.5sin(2000πt)



## Plot of VOUT and VIN

### Input Parameter:

DC signal from 0 to 5V (using offset)



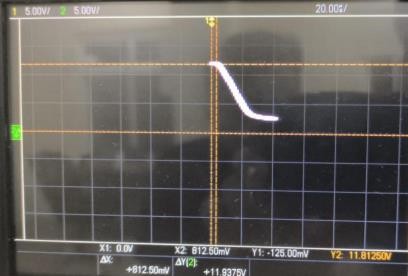
The graph has 3 parts:

1. **Cut-off Region**: First straight line part (VGS < VT)
2. **Saturation Region**: Slant region (VGS > VT and VDS > VGS – VT) 3.**Linear Region**: Next straight-line part (VGS > VT and VDS < VGS – VT)

|  |  |  |
| --- | --- | --- |
| **REGION** | **VIN** | **VOUT** |
| CUT-OFF | 812.5mV | 7.437V |
| SATURATION | 3.8125V | 11.9375V |
| LINEAR | 7.9375V | 2.8750V |

## (b) Modes Of Operation

#### Cut-Off Mode:



|  |  |  |  |
| --- | --- | --- | --- |
| **VDS** | **VIN** | **VO** | **GAIN** |
| 1V | 50mV | 11.3mV | 0.226 |
| 1V | 100mV | 16.9mV | 0.16+9 |
| 1V | 500mV | 111mV | 0.222 |
| 1V | 1000mV | 314mV | 0.314 |

***Saturation Mode:***



|  |  |  |  |
| --- | --- | --- | --- |
| **VDS** | **VIN** | **VO** | **GAIN** |
| 3.5 | 50mV | 68 | 1.36 |
| 3.5 | 100mV | 127 | 1.27 |
| 3.5 | 500mV | 611 | 1.222 |
| 3.5 | 1000mV | 1230 | 1.23 |

#### Linear Mode:



|  |  |  |  |
| --- | --- | --- | --- |
| **VDS** | **VIN** | **VO** | **GAIN** |
| 5V | 50mV | 11.7 | 0.234 |
| 5V | 100mV | 16.3 | 0.163 |
| 5V | 500mV | 140 | 0.28 |
| 5V | 1000mV | 200 | 0.200 |

A significant gain in the MOSFET may be seen when the input voltage (Vin) is substantially smaller than VDS and much smaller than 2(VGS-VTH). On one side of the operational point, however, the MOSFET enters the LINEAR mode when Vin approaches VDS. The gain fluctuates and is not constant as a result. This happens because non-uniform amplification characteristics result from the MOSFET's behaviour changing as the input voltage crosses the operational point.

It is essential to choose the MOSFET's operating point so that it stays out of the triode mode for any value of VGS, even if it changes over time, in order to prevent the previously noted problem. Making ensuring the MOSFET is always in the saturation mode is the aim. We can maintain a steady and dependable amplification without the fluctuation and non-uniformity brought on by the triode mode by carefully selecting the operational point.

#### CONCLUSION:

Gain is greater than 1 only in Saturation Region.

So, MOSFET acts as an amplifier only in Saturation Region. MOSFET does not get switched on in Cut off region.

MOSFET acts as a variable resistor in Linear region.